GLAST LAT ACD ELECTRONICS SUBSYSTEM TECHNICAL DOCUMENT	Document # ACD-TBD	Date Effective 01-13-03
	Prepared by: D. A. Sheppard	Supersedes None
Document Title **GLAST LAT ACD FREE Printed Circuit Board Design Description**		

Gamma-ray Large Area Space Telescope (GLAST)
Large Area Telescope (LAT)
Anti-Coincidence Detector (ACD)

FREE (Front End & Event Electronics)

Printed Circuit Board Design Description

FIRST DRAFT

FREE Printed Circuit Board Design Description
Table of Contents

Document Change Log

Revision	Date	Change Description	Prepared by
Initial Release	1-22-03	Initial Release of DRAFT	Dave Sheppard

1.0 Summary of this Document

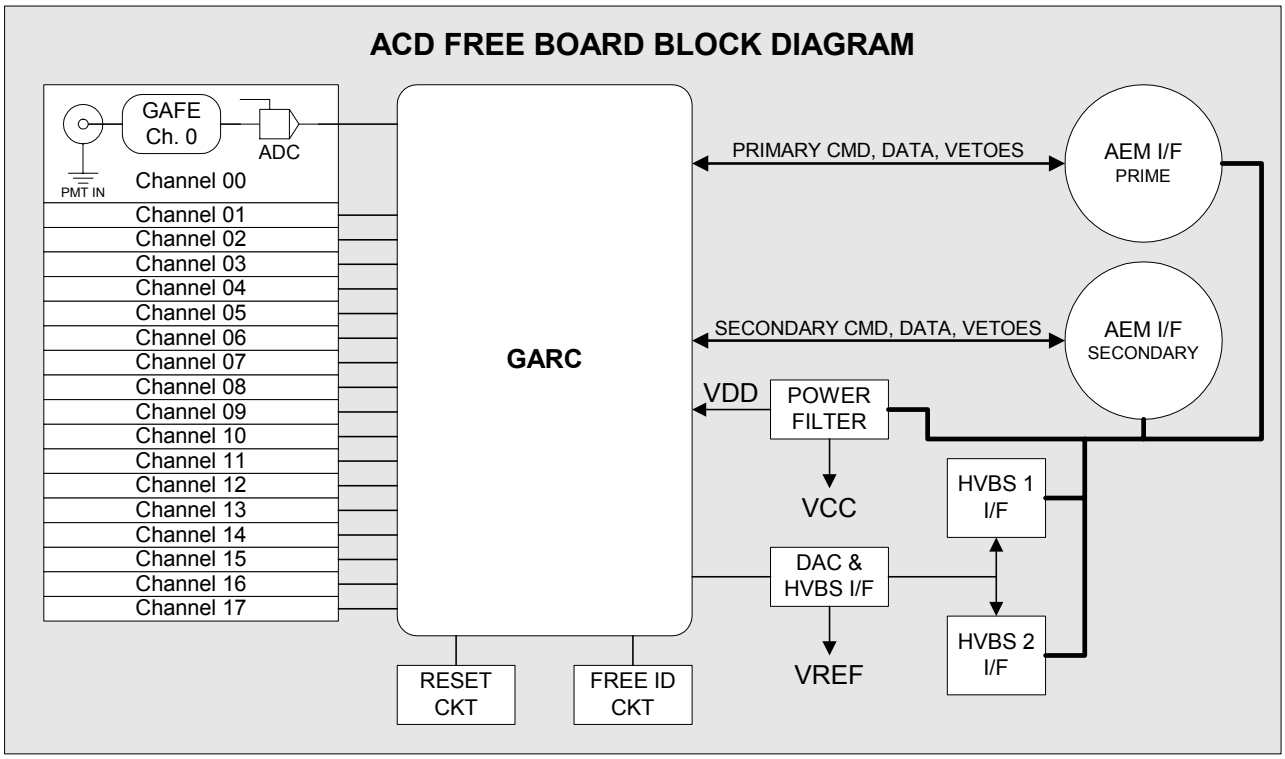
This document describes the design of the GLAST LAT ACD Front-End and Event Electronics (FREE) circuit card. The FREE PCB is designed to meet the requirements set forth in the ACD Level IV Electrical Requirements (LAT-SS-00352) and the LAT-ACD Interface Control Document (LAT-SS-00-363).

This document does not describe the functionality nor the design of the GARC or GAFE ASICs. This document describes the design and functionality of the FREE printed circuit card and depends on all parts installed on the FREE PCB to be tested as meeting requirements prior to assembly.

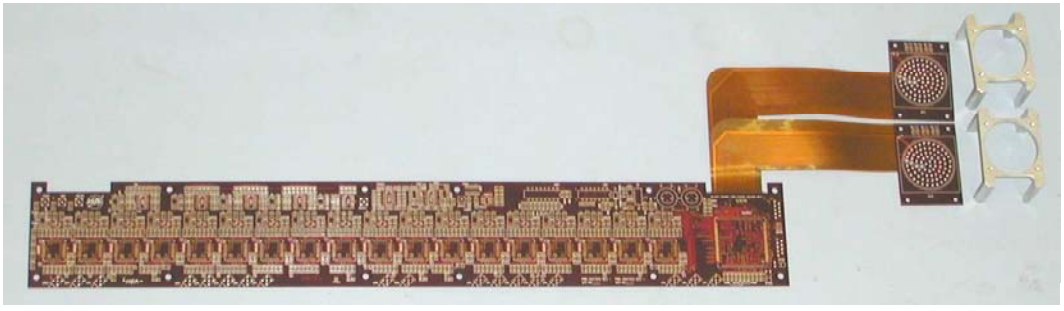
The schematics and layout are not part of this document. They may be downloaded in PDF format at the GLAST ACD website, http://lhea-glast.gsfc.nasa.gov/acd/electronics/#free

2.0 FREE Block Diagram

The following block diagram shows generically the topology of the FREE printed circuit board.



A photo of the FREE breadboard PCB is shown below



3.0 FREE Schematic Numbering

The FREE PCB schematic package consists of the following 29 pages:

Schematic Number	Schematic Name
2061840-01	FREE_TOP_SCHEMATIC
2061840-02	HVBS_INTERFACE_CIRCUITRY
2061840-03	DAC_CIRCUITRY
2061840-04	AEM_IF_PRIMARY
2061840-05	AEM_IF_SECONDARY
2061840-06	FREE_PWR
2061840-07	GARC_CKT
2061840-08	GARC_2_GAFE
2061840-09	FREE_ID_CKT
2061840-10	RST_CKT
2061840-11	ADDRESS_BUSSES
2061840-12	GAFE_CHANNEL_00
2061840-13	GAFE_CHANNEL_01
2061840-14	GAFE_CHANNEL_02
2061840-15	GAFE_CHANNEL_03
2061840-16	GAFE_CHANNEL_04
2061840-17	GAFE_CHANNEL_05
2061840-18	GAFE_CHANNEL_06
2061840-19	GAFE_CHANNEL_07
2061840-20	GAFE_CHANNEL_08
2061840-21	GAFE_CHANNEL_09
2061840-22	GAFE_CHANNEL_10
2061840-23	GAFE_CHANNEL_11
2061840-24	GAFE_CHANNEL_12
2061840-25	GAFE_CHANNEL_13
2061840-26	GAFE_CHANNEL_14
2061840-27	GAFE_CHANNEL_15
2061840-28	GAFE_CHANNEL_16
2061840-29	GAFE_CHANNEL_17

A PDF copy of these schematics may be found at: http://lhea-glast.gsfc.nasa.gov/acd/electronics/#free

4.0 FREE PCB Connectors

The FREE printed circuit card has a total of 22 connectors installed. A listing of these connectors and their function is shown below:

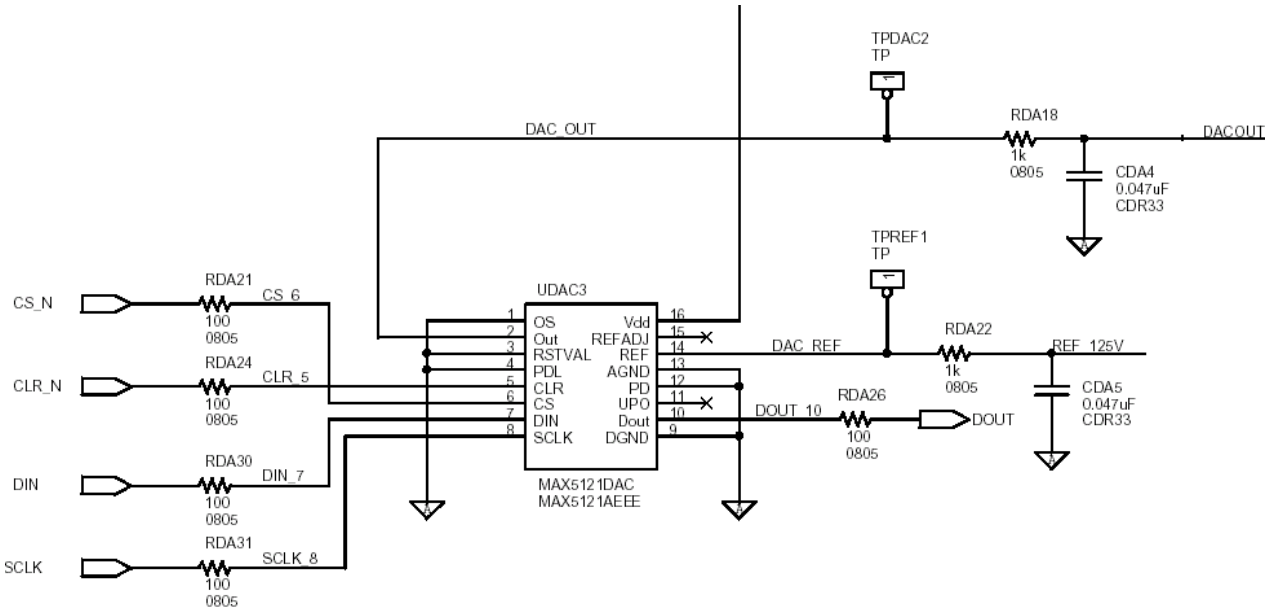
Connector Ref. Des.	Schematic Location	Connector Type	Connector Function
JP1	AEM_IF_Primary	MIL-DTL-38999, Series II, 79 pin	FREE card interface to AEM Primary
JS2	AEM_IF_Secondary	MIL-DTL-38999, Series II, 79 pin	FREE card interface to AEM Secondary
JHV1	HVBS_IF_Circuitry	MDM 9 Pin, PCB board mount	FREE card interface to HVBS Primary
JHV2	HVBS_IF_Circuitry	MDM 9 Pin, PCB board mount	FREE card interface to HVBS Secondary
J00	GAFE_Channel_00	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 00
J01	GAFE_Channel_01	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 01
J02	GAFE_Channel_02	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 02
J03	GAFE_Channel_03	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 03
J04	GAFE_Channel_04	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 04
J05	GAFE_Channel_05	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 05
J06	GAFE_Channel_06	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 06
J07	GAFE_Channel_07	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 07
J08	GAFE_Channel_08	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 08
J09	GAFE_Channel_09	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 09
J10	GAFE_Channel_10	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 10
J11	GAFE_Channel_11	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 11
J12	GAFE_Channel_12	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 12
J13	GAFE_Channel_13	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 13
J14	GAFE_Channel_14	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 14
J15	GAFE_Channel_15	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 15
J16	GAFE_Channel_16	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 16
J17	GAFE_Channel_17	Lepracon Right Angle, Threaded	PMT signal input to GAFE Channel 17

5.0 Description of the Schematic Pages

Schematic page **FREE_TOP_SCHEMATIC** is the top level schematic in the hierarchy. This top-level design ties together all the other blocks required for the board interconnect and provides a logical segmentation of the electronics. This is schematic 2061840-01.

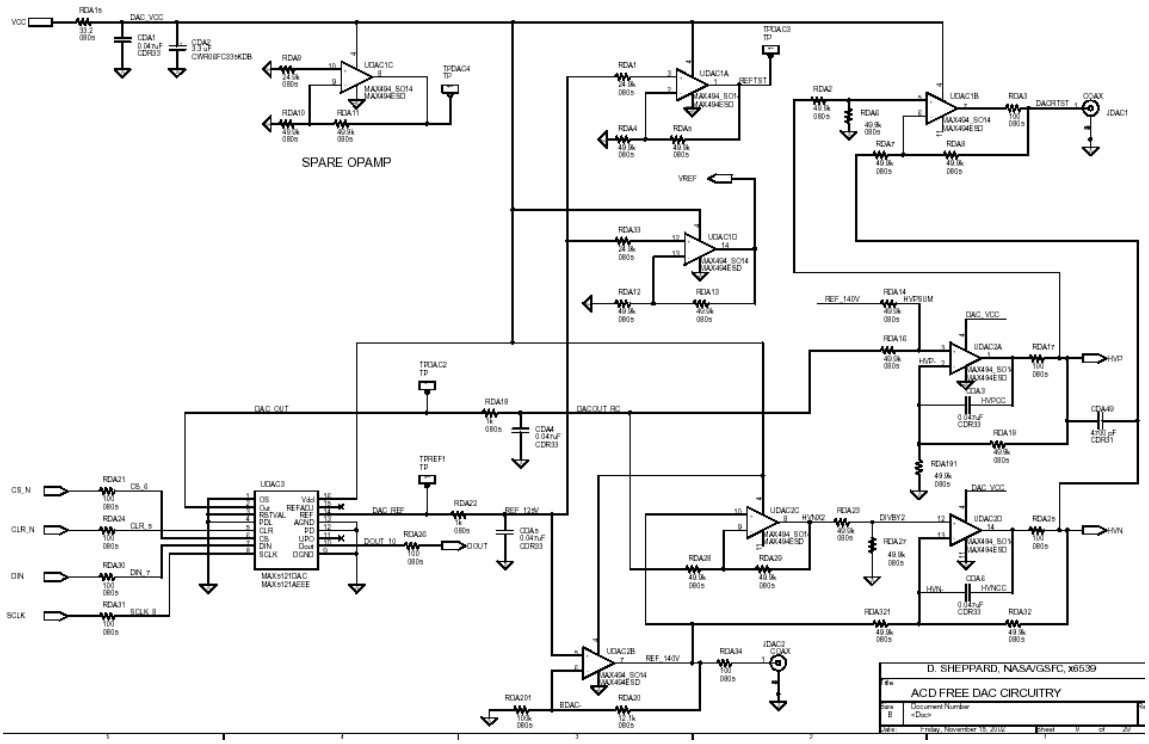
Schematic page **HVBS_INTERFACE_CIRCUITRY** contains the drawing of the two 9 pin MDM connectors that interface to the High Voltage Bias Supply. These connectors send the +28V and 28V returns to the supplies for power and the enable and analog level settings for HVBS control. A differential analog monitor is also received from each of the supplies by these connectors. This is schematic 2061840-02.

Schematic page **DAC_CIRCUITRY** contains the MAX5121 Digital-to-Analog Converter (DAC) and the associated MAX494 operational amplifiers necessary to convert the HVBS level control to a differential analog signal. This is the main discrete analog circuitry on the FREE PCB and PSPICE simulations are included later in this document.

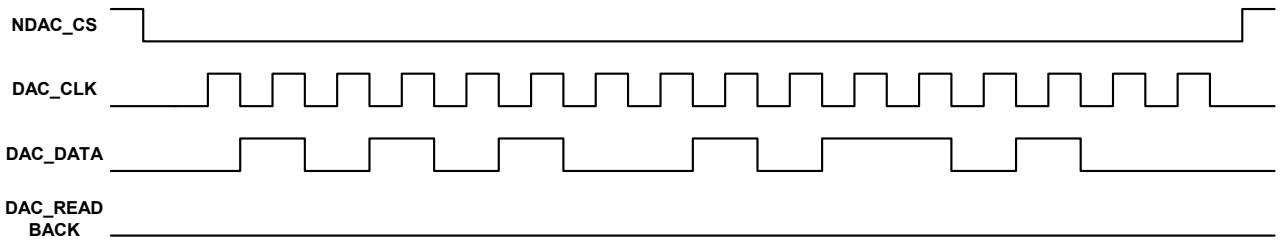


Series resistors are used between the GARC and the DAC inputs. The DAC output and reference outputs are filtered by the single RC filter shown in the schematic above.

The differential outputs, HVN and HVP, are generated by the circuitry shown on page 3 of the schematics (this is shown below with a degraded resolution). A pedestal of approximately 1.40V is generated to offset the amplifier baselines to enable operation with a single supply amplifier as the differential receiver. Simulations of this circuitry are included in section 6 of this document.



The MAX5121 DAC digital inputs driven at CMOS levels directly from the GARC ASIC. The expected control pattern is shown below.



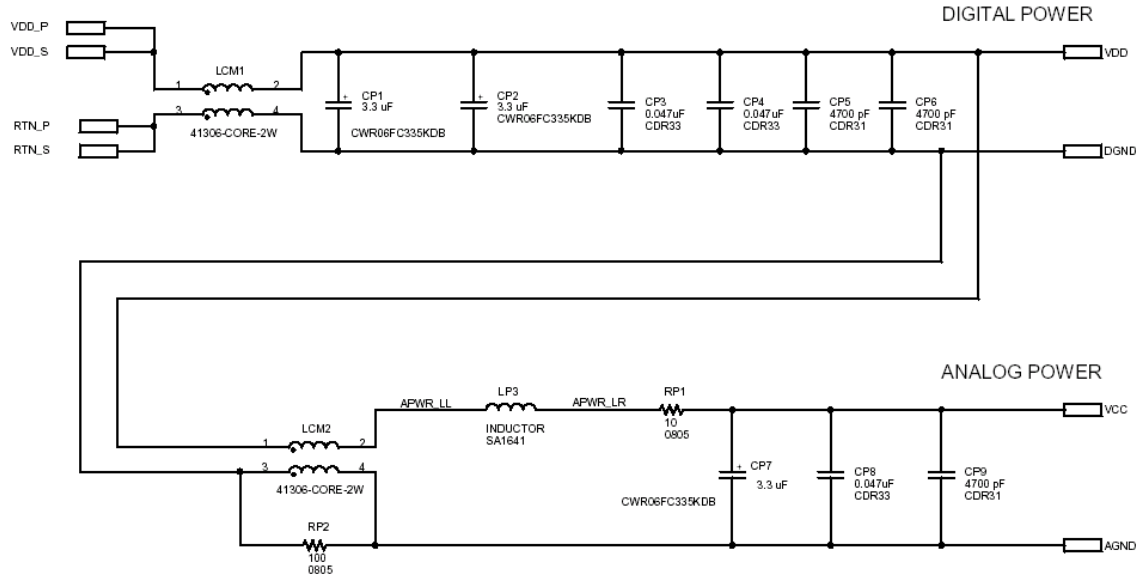
DAC DATA WRITE WITH DATA PATTERN HEX A5A

Details on the operation and control of the DAC can be found in the GARC V1 Test Report (available on the ACD website). This is schematic 2061840-03.

Schematic page **AEM_IF_PRIMARY** and **AEM_IF_SECONDARY** contain the drawings for the Series II circular connectors that interface to the LAT. These drawings are identical except for the component reference designators. The pin locations are fixed as per the ACD-LAT Interface Control Document. These schematics also contain termination resistors for the LVDS receivers, thermistors, and a 33Ω resistor between 28V Return and the +3.3V Return. Nominally, these returns are tied together in the LAT GASU, but are tied here for safety during bench level testing, anticipating the possibility of incorrectly wired EGSE. This precludes the possibility of 28V Return floating relative to +3.3V Return and inadvertently presenting an over-voltage condition to a FREE component. These are schematics 2061840-04 and –05, respectively.

Schematic page **FREE_PWR** contains some power conditioning for the FREE electronics. Note that the FREE card does not use the +28V supply, but rather is just a conduit for the HVBS to receive this

voltage. The FREE card operates on a single +3.3V power rail. The +3.3V input and +3.3V return enter the power and pass through a common mode choke.



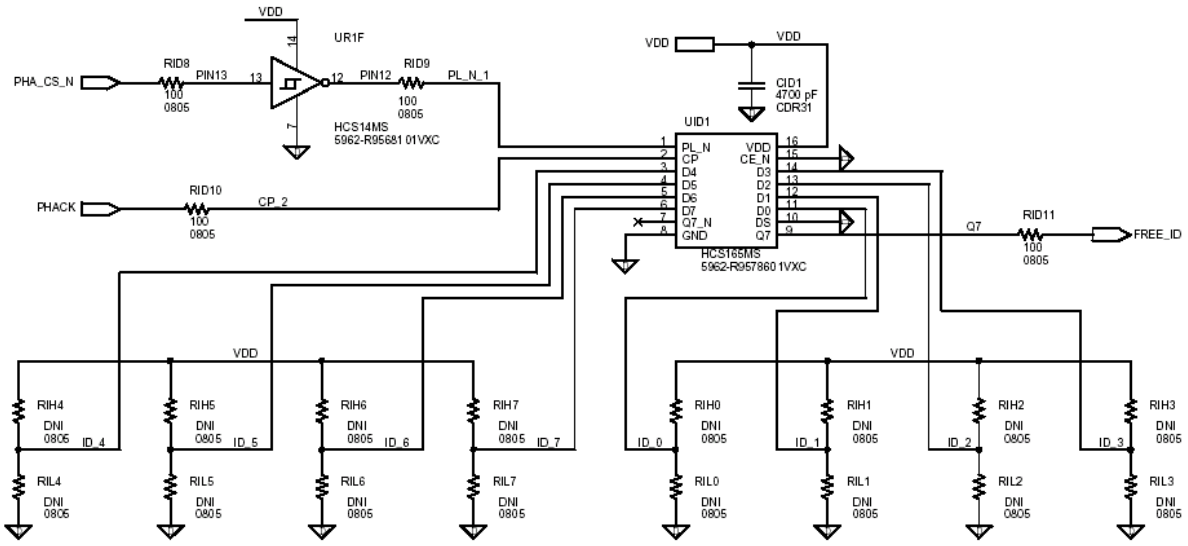
This common mode choke has been custom-built for ACD as per Goddard specification S-311-320-LATACD-0004. It has a value of approximately 0.6 mH. The principle of using the common-mode inductive filter is that the DC 'power line' flux will ideally sum to zero (i.e., cancel) due to the opposing nature of current in moving in the opposite direction of the return current. Alternately, flux that is common mode, such as AC noise, is left unopposed and therefore encounters the high reactive impedance of the core material. The idea is that this high impedance offers filtering action against the common mode noise. In the FREE circuit, it is used in conjunction with filter capacitors, both tantalum and ceramic. A second filter setup in a similar way is used to provide AC-isolation between the analog and digital circuitry of the FREE PCB. It is possible that the inductor LP3 will be omitted from the final flight design if it introduces either excessive series impedance or is found to be unnecessary. SPICE simulations of the expected performance are shown later in this document. This is schematic 2061840-06.

Schematic page **GARC_CKT** contains the drawing of the GLAST ACD Readout Controller (GARC) 208 pin digital ASIC and hierarchically links to the power-on reset circuit and the FREE board identification circuit. This schematic also has the associated GARC digital power bypass capacitors and places for additional GARC biasing resistors. Nominally, the GARC biasing is setup internally, but these on-board resistors allow for bias current adjustment after ASIC fabrication. This is schematic 2061840-07.

Schematic page **GARC_2_GAFE** contains the hierarchical interconnection path for connection of the FREE GARC (1 per board) to the front-end GAFE ASICs (18 per board). Additionally, common termination resistors are placed on this schematic as well as some test points. This schematic also has a hierarchical connection to the GAFE address busses. This is schematic 2061840-08.

Schematic page **FREE_ID_CKT** contains a discrete shift register (HC165MS) and address resistors which are to be used to provide each FREE PCB with a unique serial number. The shift register is required serialized the address data due to a lack of I/O pins available on the GARC. The scheme for FREE PCB serialization is given in the table below. This is schematic 2061840-09.

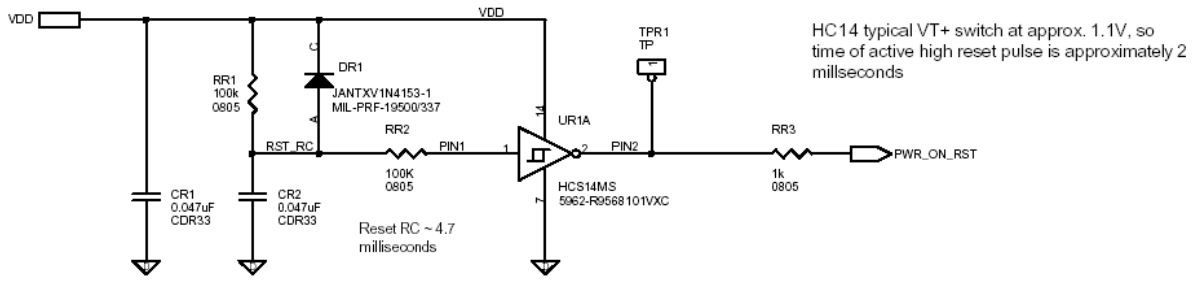
FREE Board ID Bits	Description	Pattern Code
Bit 7	PCB Status Bit (reserved)	0: Nominal Code for FREE PCBs 1: Reserved for use by Design Engr.
Bits [6:5]	PCB Status Designator	2'b00: FREE PCB Breadboard (BB) Version 2'b01: FREE PCB Engineering Model (EM) Version 2'b10: FREE PCB Flight Model 2'b11: Reserved
Bits [4:0]	Board Serial Number With values 0x0 to 0x1F	Serial number indicates order of assembly as per GSFC WOA. This is defined by the Design Engr. at the time the WOA is generated.



FREE Board ID Circuit

The HC165MS is a radiation-hardened silicon-on-insulator part. This has been tested in the lab to work over temperature down to a voltage of 1.5V DC.

Schematic page **RST_CKT** contains a resistor-capacitor network with a schmitt-trigger inverter to generate a power-on reset. The inverter, HC14MS, should have a threshold in the area of 1.1V. With the resistor-capacitor combination specified, this should provide an active-high reset pulse, PWR_ON_RST, of approximately 2 milliseconds. The timing on this is not critical within an order of magnitude. This is schematic 2061840-10.

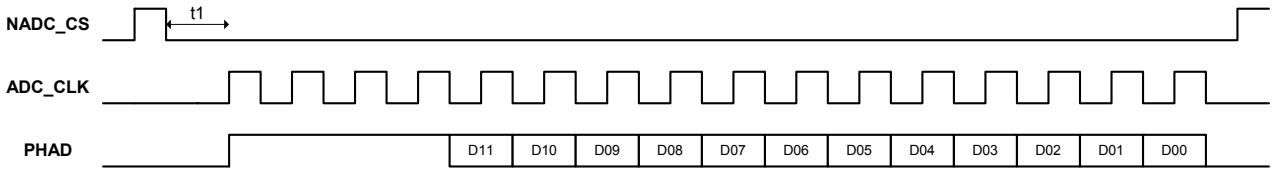


Series resistors are provided at the inverter input and output to provide isolation from noise/glitches. The diode DR1 is provided to discharge capacitor CR2 when the FREE circuit is powered off. The HCS14MS part is a radiation-hardened silicon-on-insulator part. This circuit has been tested functional in the lab operating over temperature down to 1.4 volts.

Schematic page **ADDRESS_BUSSES** contains the pull-up and pull-down resistors necessary to provide each of the 18 GAFE ASICs with a unique digital address. The digital address corresponds to the PMT input connector designator, the GAFE reference designator, and ADC reference designator. This is schematic 2061840-11.

Schematic pages **GAFE_CHANNEL_00** through **GAFE_CHANNEL_17** contain the individual analog channel circuitry. Each of these schematics is identical with the exception of reference designators. Each GAFE channel contains the input connector, input termination network, GAFE ASIC, MAX145 ADC, and the voltage reference buffering circuitry. Additionally, the bypass circuitry for each analog channel is shown here. These are schematics 2061840-12 through -29.

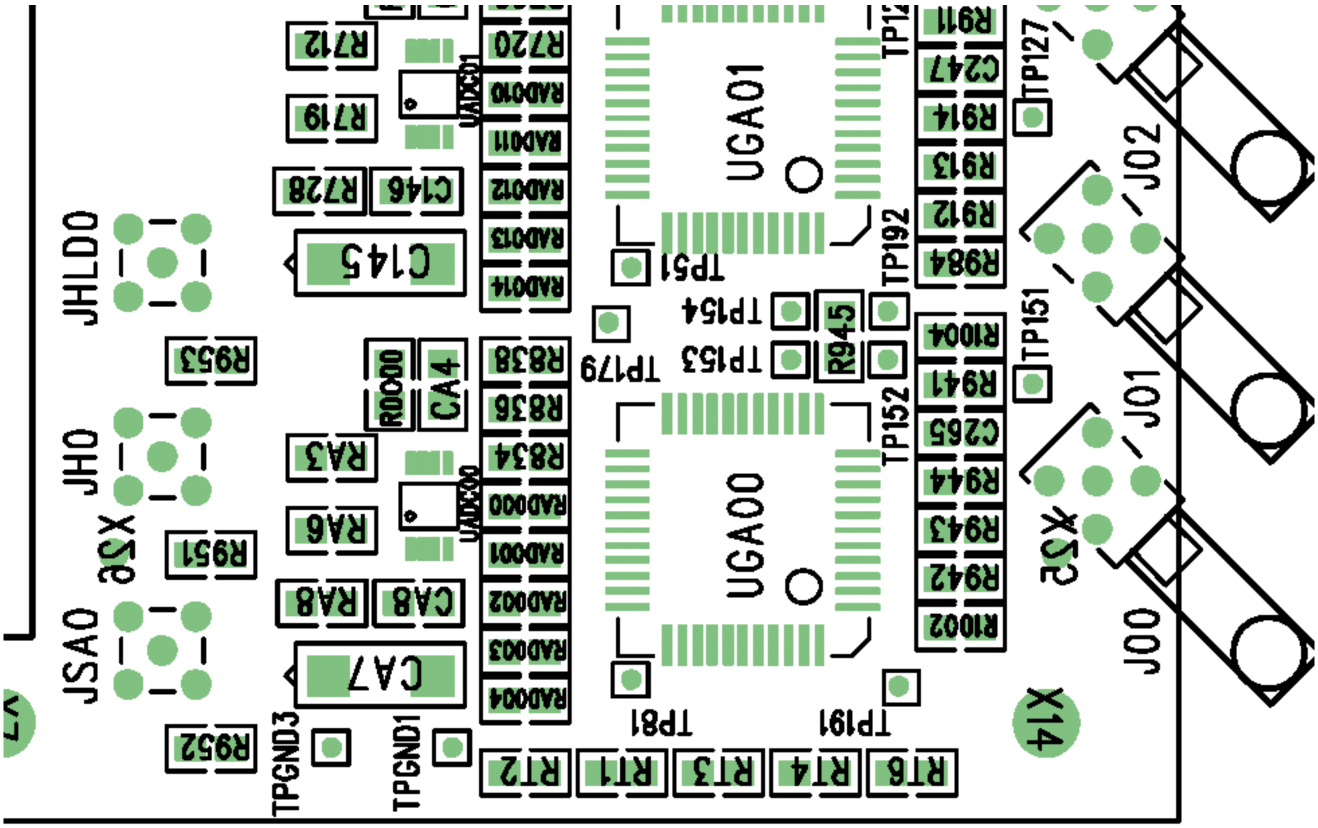
The MAX145 digital inputs are driven at CMOS levels directly from the GARC ASIC. The expected control pattern is shown below.



MAX145 ADC CONVERSION CYCLE

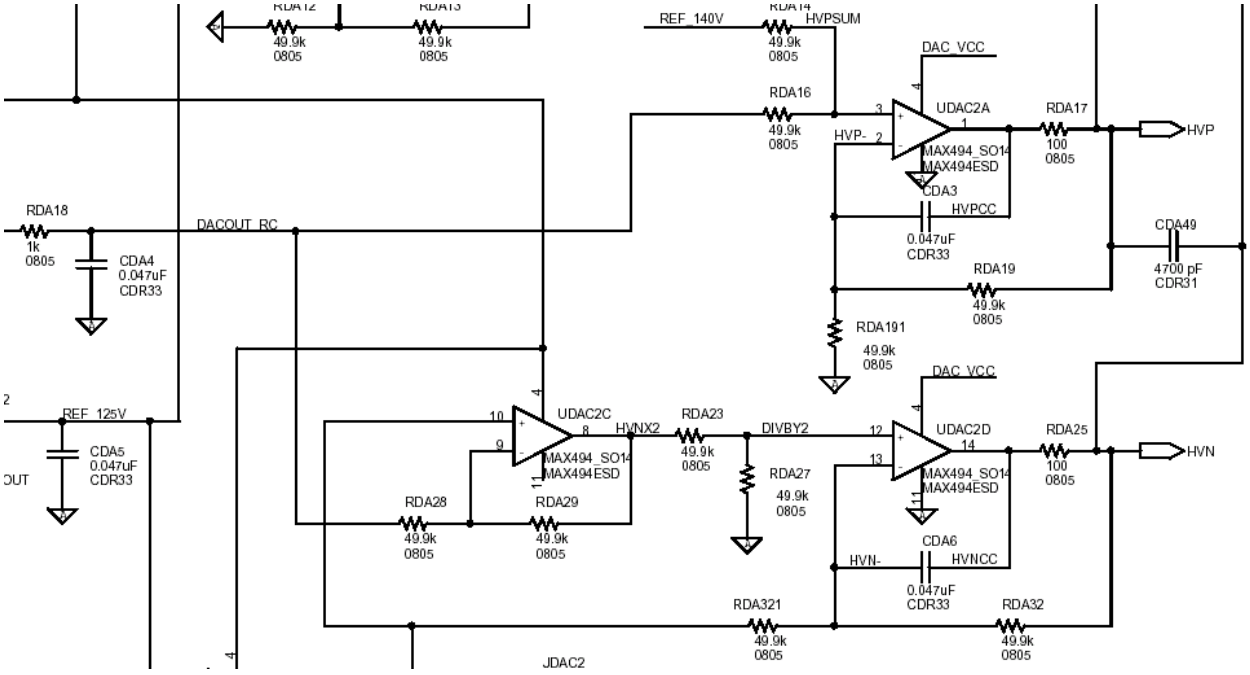
Series resistors are used between the GARC and the ADC inputs. Details on the operation and control of the ADC can be found in the GARC V1 Test Report (available on the ACD website).

The assembly drawing for the top of the board, GAFE channel 00, is shown below. There are few passive components on the back of the board. The ADC is in close proximity to the GAFE by design, as are the input connector and charge-splitting network.

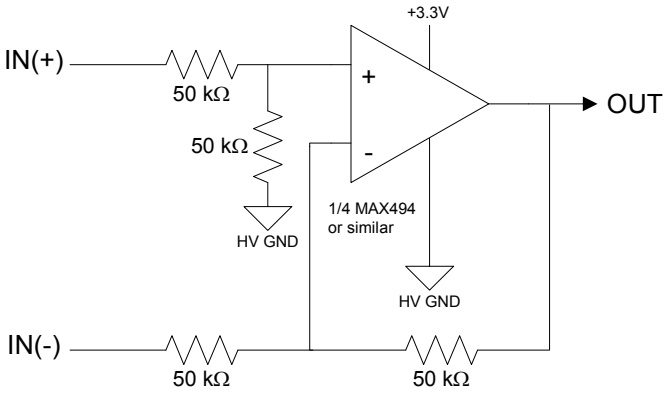

JHLD0
JH0
JSA0
R953
R951
R952
TPGND3
TPGND1
R712
R719
R728
C146
C145
R0C00
CA4
RA3
RA6
RA8
CA8
CA7
UADC01
UADC00
R720
RAD010
RAD011
RAD012
RAD013
RAD014
R838
R836
R834
RAD000
RAD001
RAD002
RAD003
RAD004
RT2
RT1
RT3
RT4
RT6
UGA01
UGA00
TP51
TP179
TP154
TP153
R945
TP81
TP191
TP192
TP152
TP151
TP127
R911
C247
R914
R913
R912
R984
R1004
R941
C265
R944
R943
R942
R1002
J00
J01
J02
X14

6.0 HVBS Receiver – Calculations and PSPICE Simulation

The circuitry on the FREE card that is driving the differential analog outputs to the HVBS receiver is as follows:



A sample circuit for the expected HVBS receiver is shown below. This has been simulated in PSPICE (with corresponding calculations performed via spreadsheet). The results are presented below.

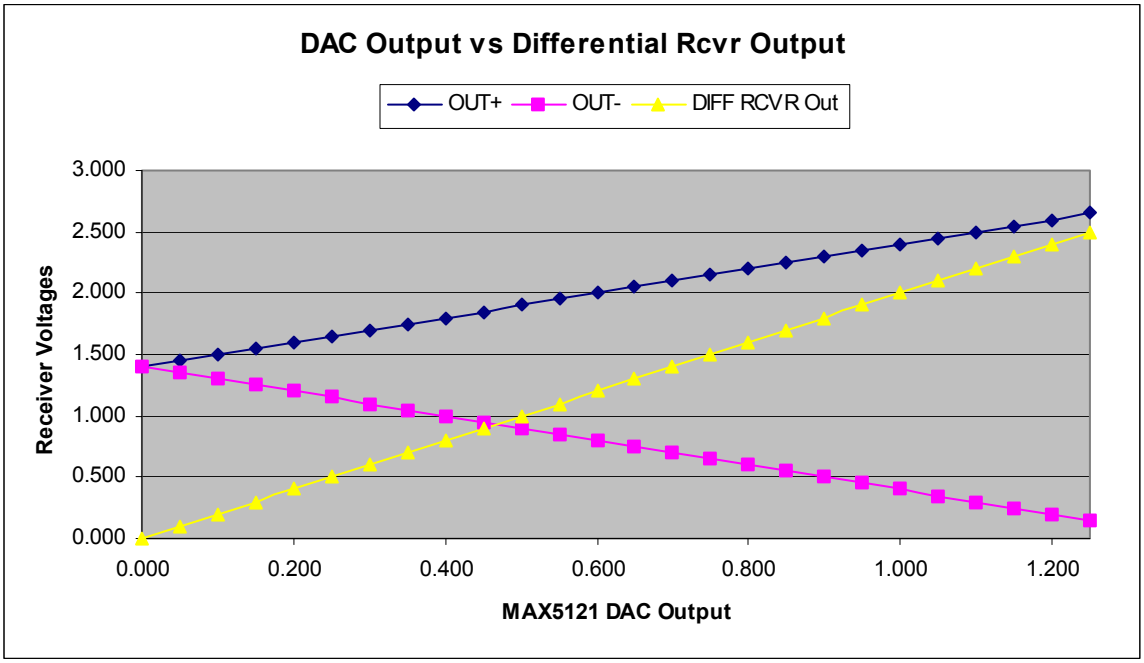


Differential Receiver Circuit Example

The following chart lists the expected HVP (IN+), HVN (IN-), and OUT voltages for the ideal differential receiver using the FREE circuit 1.4V pedestal offset.

DAC_OUT	OUT+	OUT-	DIFF RCVR Out
0.000	1.400	1.400	0.000
0.050	1.450	1.350	0.100
0.100	1.500	1.300	0.200
0.150	1.550	1.250	0.300
0.200	1.600	1.200	0.400
0.250	1.650	1.150	0.500
0.300	1.700	1.100	0.600
0.350	1.750	1.050	0.700
0.400	1.800	1.000	0.800
0.450	1.850	0.950	0.900
0.500	1.900	0.900	1.000
0.550	1.950	0.850	1.100
0.600	2.000	0.800	1.200
0.650	2.050	0.750	1.300
0.700	2.100	0.700	1.400
0.750	2.150	0.650	1.500
0.800	2.200	0.600	1.600
0.850	2.250	0.550	1.700
0.900	2.300	0.500	1.800
0.950	2.350	0.450	1.900
1.000	2.400	0.400	2.000
1.050	2.450	0.350	2.100
1.100	2.500	0.300	2.200
1.150	2.550	0.250	2.300
1.200	2.600	0.200	2.400
1.250	2.650	0.150	2.500

Or, graphically as,

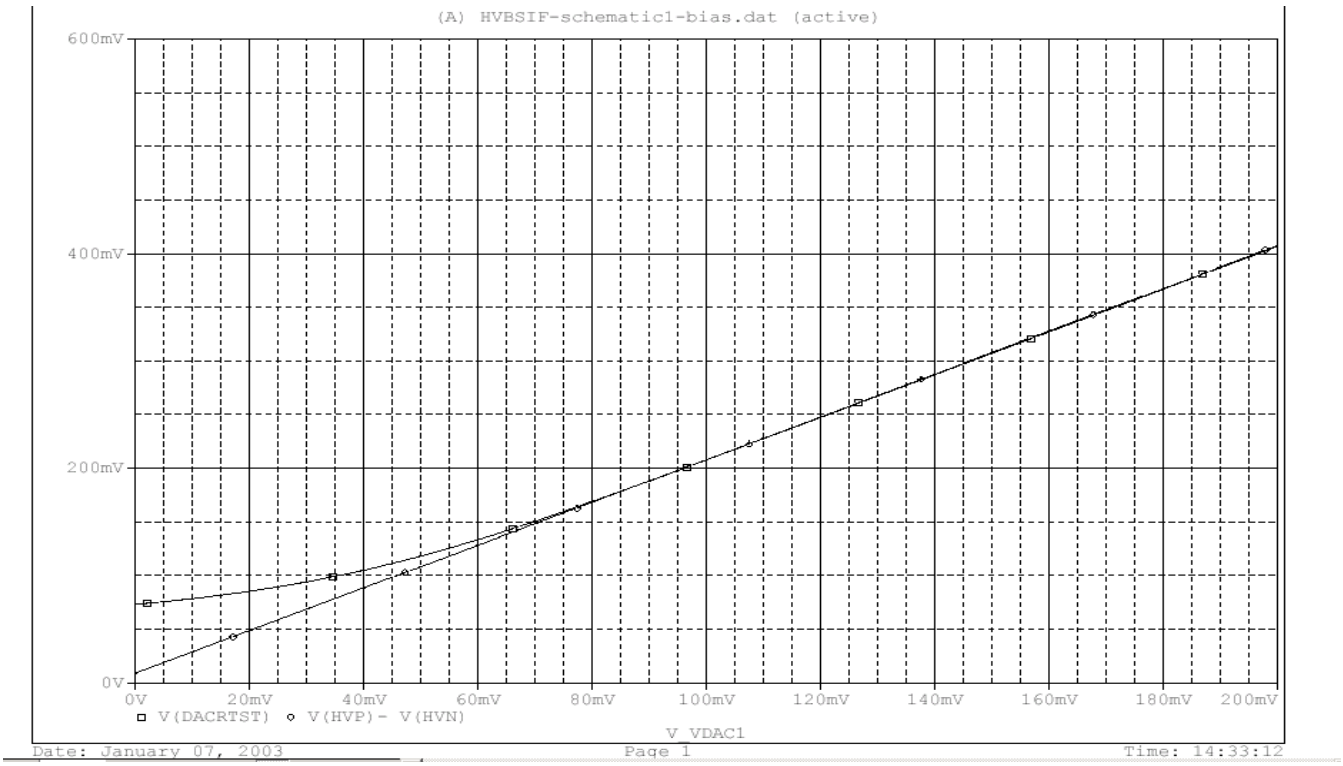


The important point to this graph is that the voltages from the FREE card, OUT+ and OUT-, are maintained away from the power rails during the entire range of DAC operation. This allows for linear operation using a single +3.3V rail.

A SPICE simulation of the circuit shows similar results to ideal with the exception of a non-linearity near the bottom of the HVBS output range. This is due to the use of a single supply receiver and is not a problem in ACD operations.

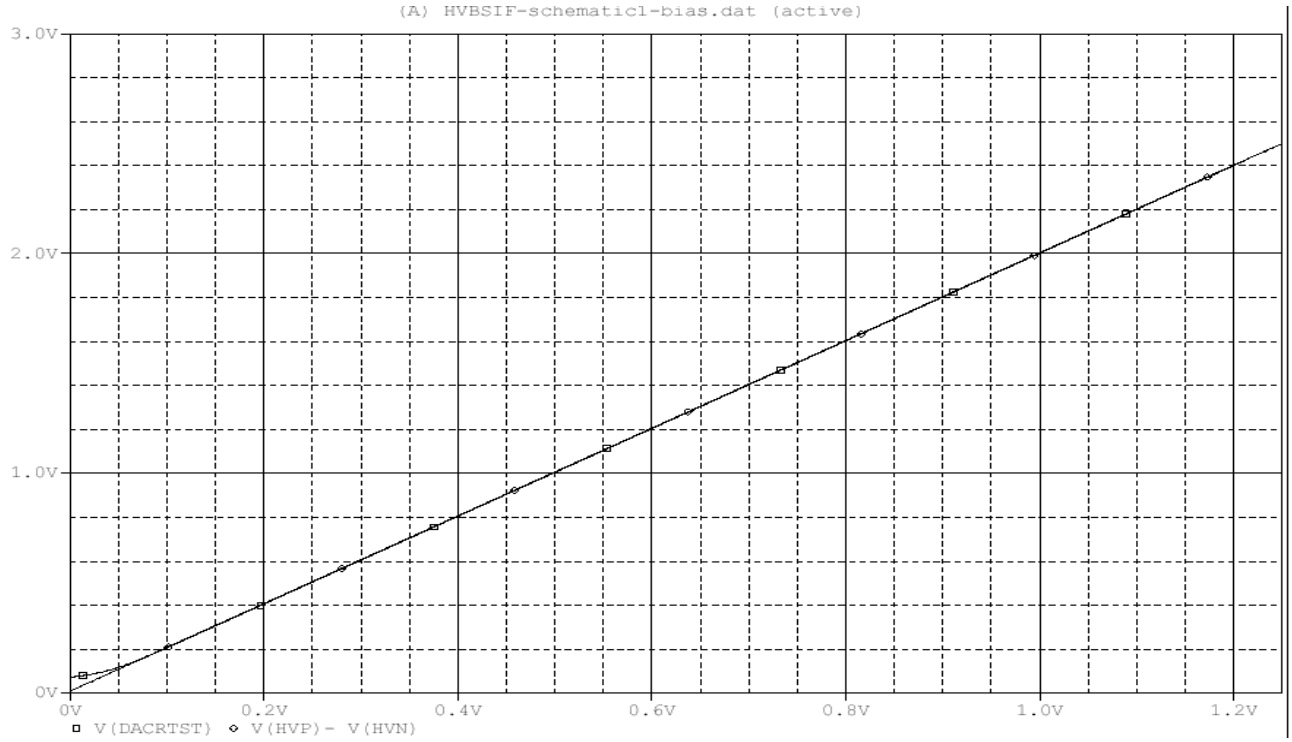
Specifically, the ACD HVBS needs to operate in the range of 400V to 1310V with a differential received voltage of 0 to 2.50V. This gives the V(HV_Out) / V(DAC_In) transfer function to be 1310/2.50 or 5.24 V / mV. This requires the differential receiver to be linear with an output above (400 / 5.24) mV = 76 mV. This is shown in the SPICE plots below.

For differential voltages below 80 mV, the output experiences a non-linearity as the MAX494 opamp cannot drive the output all the way to the negative rail. The SPICE simulation following demonstrates this effect.



SPICE Plot Zoom of Receiver Amplifier Non-Linearity below 80 mV on the DAC Output

Looking at the full range of the differential receiver, the output is linear from the 0.08 V to 1.25V range. This encompasses a linear range on the HVBS output of 85V to 1310V.



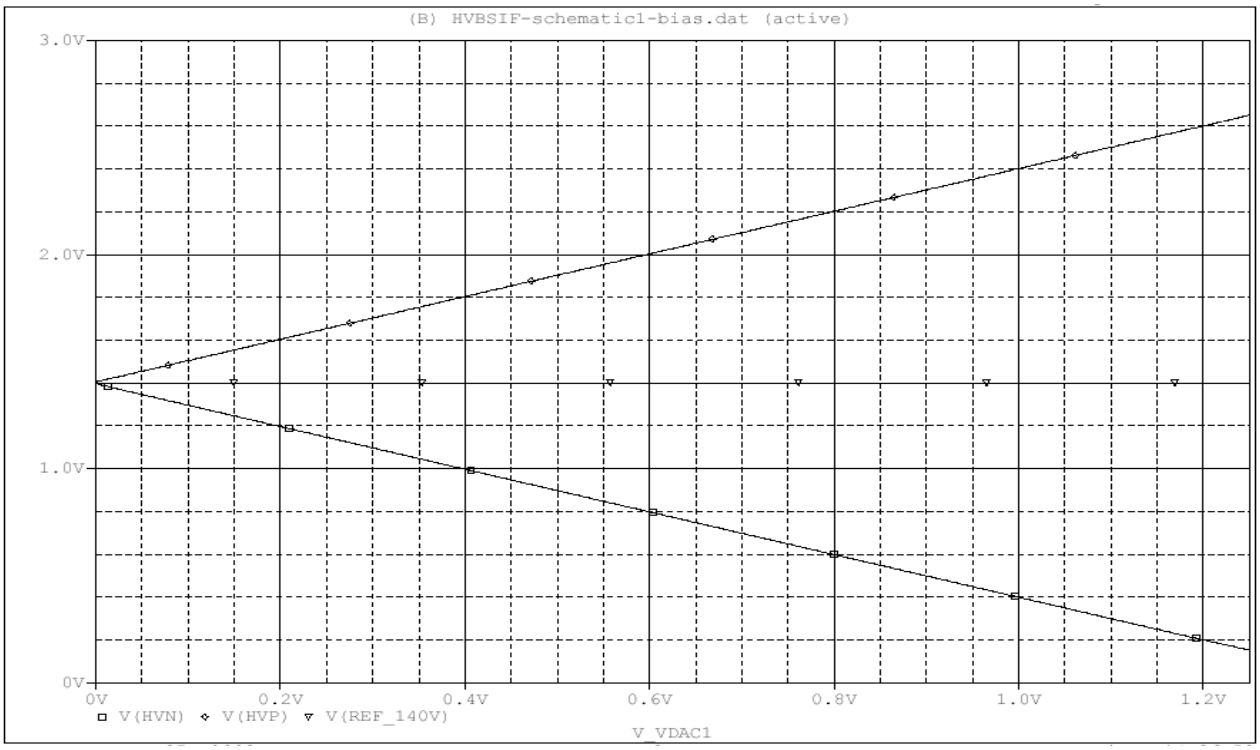
SPICE Plot of the Differential Input vs. Receiver Output Voltages for a single-supply opamp receiver

This SPICE plot shows the two differential voltage outputs, HVP and HVN, for a DAC output voltage from 0 to 1.25V. The REF_140V pedestal voltage is also plotted. This plot details the range the range of the signals as follows:

HVN = REF_140V – DACOUT
HVP = REF_140V + DACOUT

And the differential receiver output is:

RCVR_OUT = HVP – HVN = (REF_140V + DACOUT) – (REF_140V – DACOUT) = 2 *DACOUT

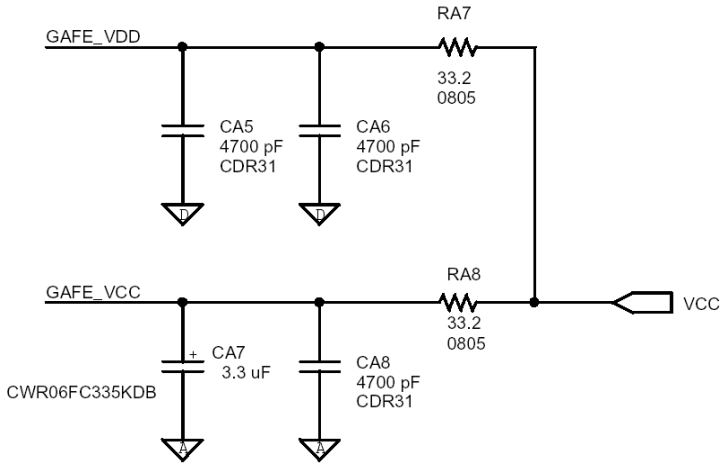


SPICE plot of HVN (Out-), HVP (Out+), and the 1.40V Pedestal Reference

7.0 Design of the GAFE Channel Section

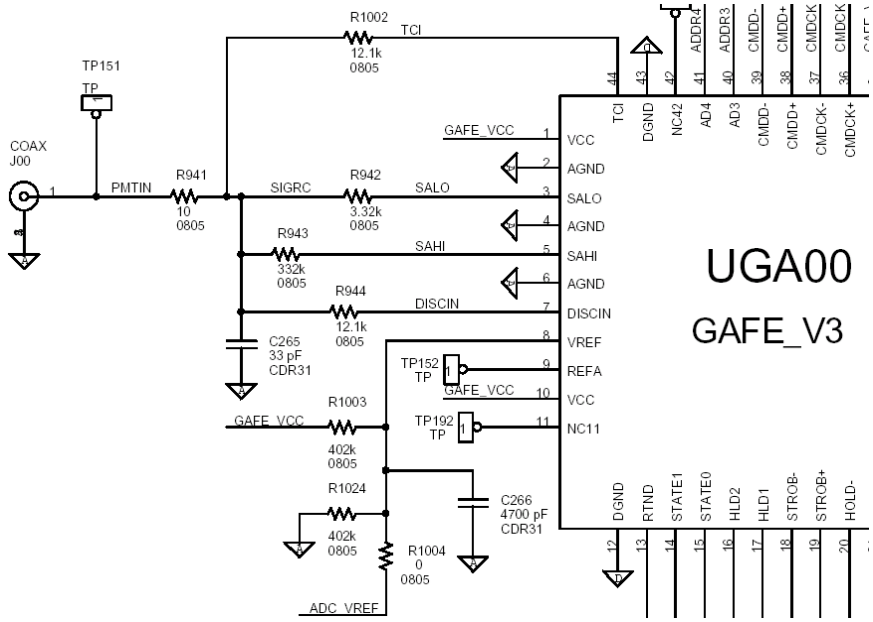
The FREE PCB is designed to support 18 GAFE ASICs. The PCB is required to provide the substrate necessary to bring the signal into the GAFE from the phototube through a defined input network, provide a voltage reference, provide digital controls and interface to the GARC, and provide an analog to digital converter. Power filtering is also provided.

Each GAFE nominally draws about 2 mW on the digital power supply (GAFE_VDD) and 4 mW on the analog power supply (GAFE_VCC). Each power supply plane has a 33.2 Ω series resistor between the plane and the GAFE ASIC, providing an expected drop of about 40 mV between the plane and the ASIC. There are also ceramic and tantalum bypass capacitors to provide isolation between the supplies.



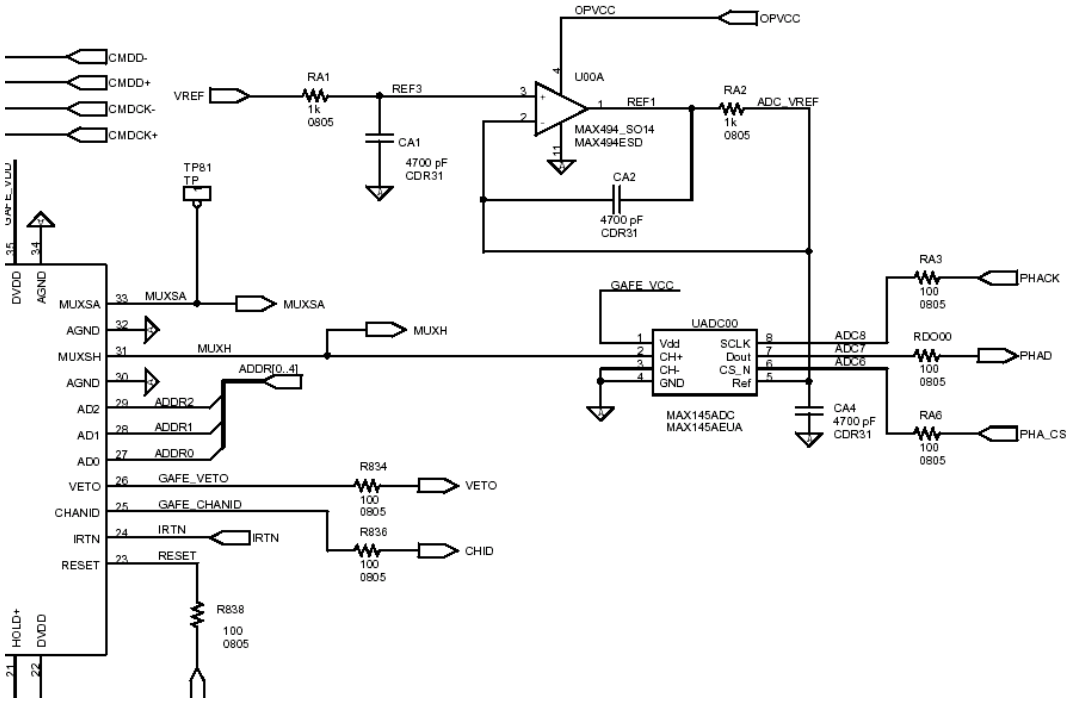
This provides noise isolation and some margin of safety should one of the analog channels experience and increase in noise and/or current.

The front-end input for the GAFE ASIC is detailed in the diagram below. The approx. 100:1 charge splitting network can be seen with the 332 kΩ resistor input to SAHI and the 3.32 kΩ resistor input to the SALO pin. The discriminator input, DISCIN, and the test charge injection circuit, TCI, both have 12.1 kΩ resistors as interconnects. The Lepracon coaxial input connector is shown at the left and a 100V 33 pF capacitor is used to integrate the charge from the input signal. The time constant from the input network is then 33 pF x 12.1 kΩ = τ = 400 nsec. The voltage reference is bypassed with a 0705 ceramic capacitor close to the ASIC pin.



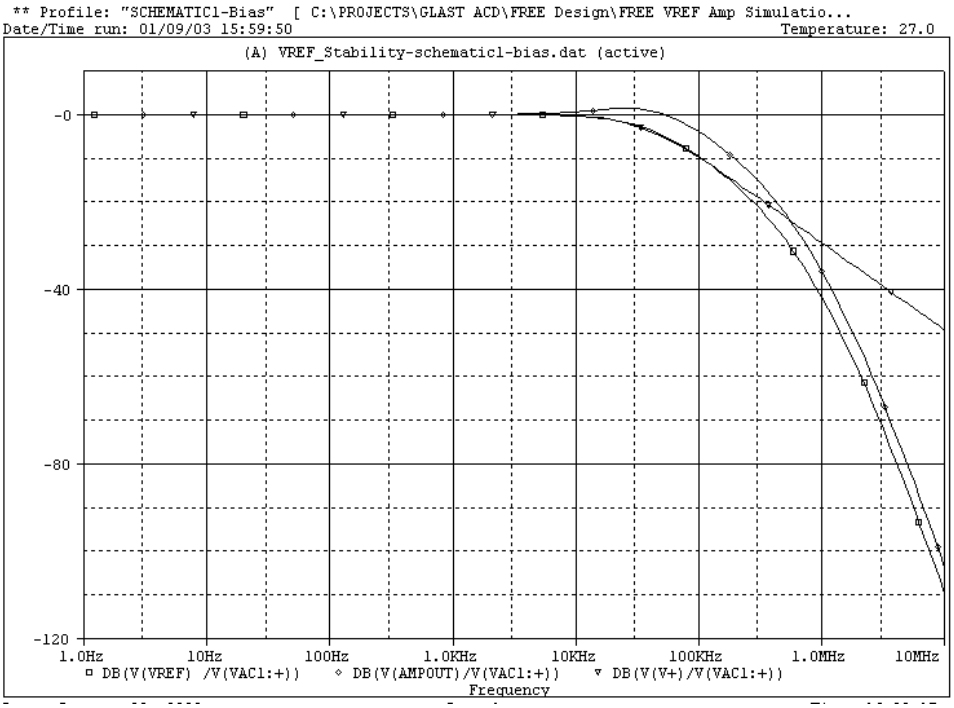
GAFE Input Network

The interface from the GAFE to the MAX145 ADC is shown below.

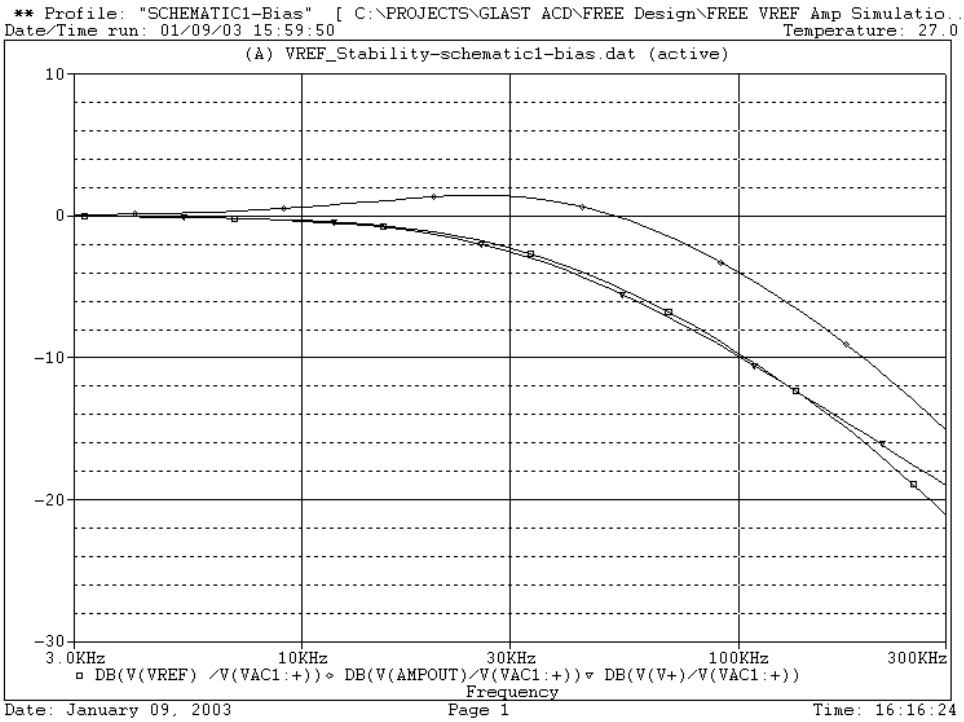


The GAFE drives the MAX145 ADC directly from the held shaping amplifier pin, MUXSH. The ADC is less than 10 mm from the ASIC. The voltage reference to the ASIC and ADC is buffered and bypassed with two capacitors (one close to the ASIC input, one close to the ADC input). The ADC digital control lines, which are CMOS levels, are isolated via 100 Ω series resistors.

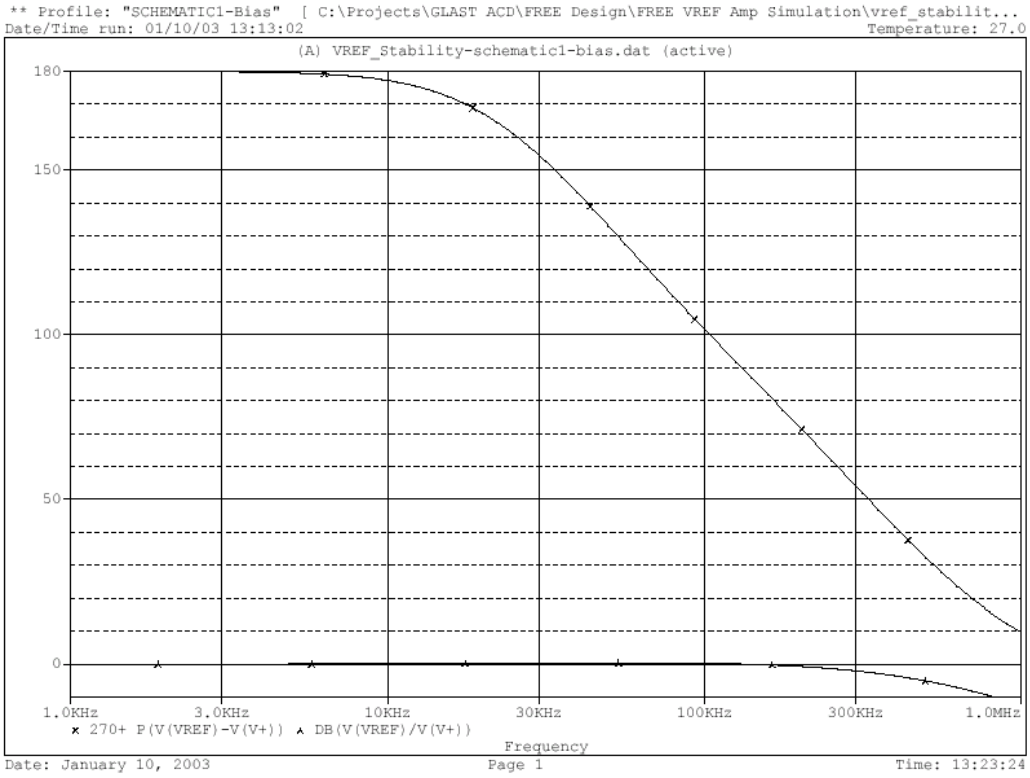
The AC noise rejection of the voltage reference buffer (shown as U00A) is shown in the SPICE simulation plot below.



The three traces show the amplifier input, amplifier output, and VREF nodes. The RC at the amplifier input provides the 20 dB/decade rolloff shown. The amplifier output shows a slight peaking near 30 kHz. The VREF shows a smooth rolloff above the cutoff frequency. A zoom of this feature is shown below.



Checking the phase margin in simulation for this circuit in the plot below,

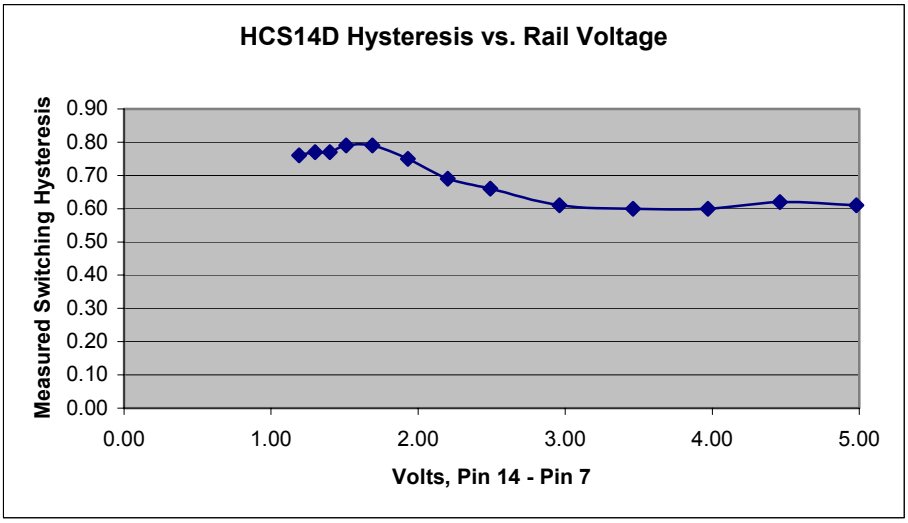


GAFE/ADC VREF phase margin simulation

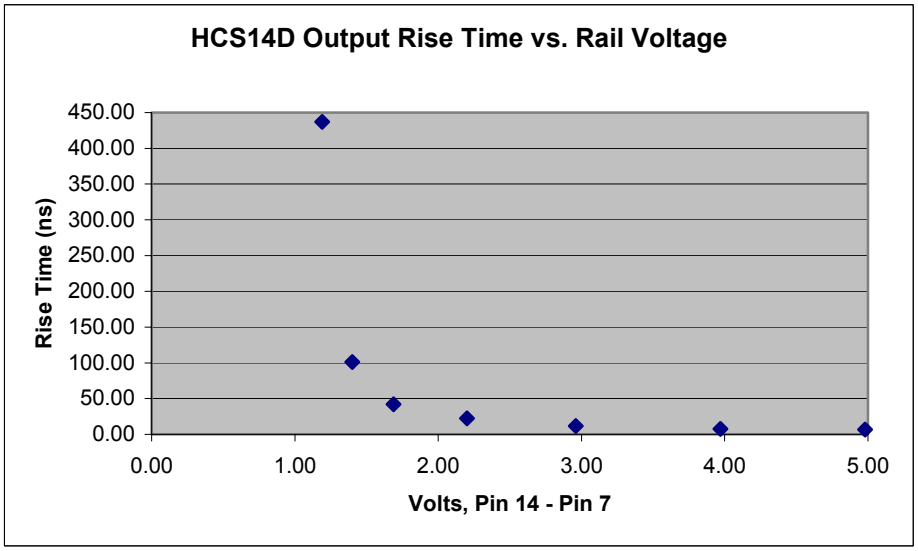
The buffer is a unity gain setup. The –3dB point of the filter is at 363 kHz. We measure the phase margin of the buffer at this point as 46 degrees, which demonstrates a stability margin. At 100 kHz, the phase margin is measured at 101.5 degrees.

8.0 Test Results of the HCS14 and HCS165 at Lower Voltages

The FREE PCB operates on a single +3.3V rail. It uses two discrete logic parts, the HCS14 and the HCS165, for the reset and FREE board identification number circuits. While commercial HCMOS logic is specified for operation down to +2.0V, the Class S HCS parts are only characterized between +4.5V and +5.5V. The following test was performed to verify operation in the expected range of the FREE board power, which is +3.0V to +3.6V. It was found that the HCS parts operate to below +2.0V (although performance is degraded in this region). Since the FREE board is designed to operate down to a minimum of +3.0V, these parts will operate with margin in this range. Two of the HCS14 inverting gates were connected to form an oscillator (68 kΩ resistor between pins 1-2, 0.01 µF capacitor between pins 1-4) and the rise time and period were measured. The HCS165 was clocked with this oscillator for the parallel load and a 4 MHz clock used for readout. The HCS14 oscillator functioned at room temperature down to 1.07V. In thermal tests, the performance was slightly better when warm and degraded to 1.26V cold. A summary of the results is shown below.



Hysteresis was measured by monitoring the switching points on the HCS14 and defining $V_{HYS} = V_{TH} - V_{TL}$



9.0 FREE Parts Selection

The FREE printed circuit board has a variety of passive and active parts that have been selected in view of the specific requirements of the LAT instrument. A table summarizing the various part choices is listed below.

Part Type	Approximate Number Used	Reason For Selection	Alternate Choices / Second Sources
GARC ASIC	1	Full-custom ACD-specific ASIC	N/A
GAFE ASIC	18	Full-custom ACD-specific ASIC	N/A
MAX145 ADC	18	Same part being used on LAT Calorimeter	N/A
MAX5121 DAC	1	Same part being used on LAT Calorimeter	N/A
MAX494 opamp	6	Parts in screening at GSFC now prior to flight approval	-
MIL-PRF-55681 Ceramic Capacitors	175	Approved for Flight on the NASA Parts Selection List	Several manufacturers available
MIL-PRF-55365 Tantalum Capacitors	25	Approved for Flight on the NASA Parts Selection List	Several manufacturers available
HCS14MS	1	Approved for Flight on the NASA Parts Selection List	54HC14
HCS165MS	1	Approved for Flight on the NASA Parts Selection List	54HC165
MIL-PRF-55342 thick film resistors	500	Approved for Flight on the NASA Parts Selection List	Several manufacturers available
1N4153 diode	1	Approved for Flight on the NASA Parts Selection List	1N4150
Lepracon Coax	18	Approved for Flight	-
MDM-9 pin connector	2	Approved for Flight on the NASA Parts Selection List	Several manufacturers available
MIL-DTL-38999 Series II Circular connector	2	Approved for Flight on the NASA Parts Selection List	Several manufacturers available
Common-Mode filter inductor	2	Approved for Flight – manufactured per GSFC S311 specification	-
Thermistor	2	Approved for Flight – manufactured per GSFC S311 specification	-

10.0 FREE PCB Design

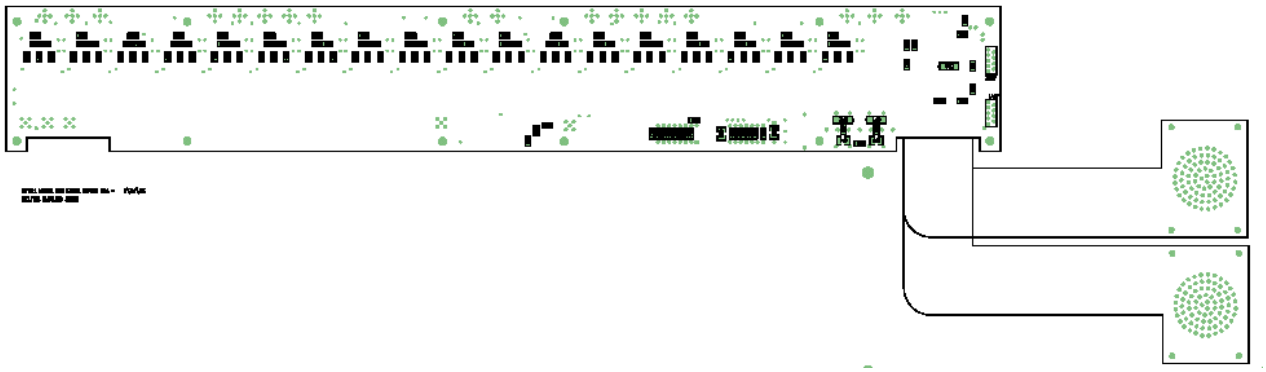
The FREE printed circuit board is a 10 layer flexible-rigid circuit board fabricated to the IPC 6013 Type 4 Class 3 standard. The material type is a combination of rigid polyimide and kapton flex per IPC4101/40 and IPC-FC-241. The finished board thickness is 0.062", +/- 0.007". The kapton flex layers are finished to 0.008", +/- 0.003" over the cover film, which exists for both flex sides. There is a liquid photo-imageable soldermask on both sides of the board. All corners are radiused to 0.062" to preclude handling damage to the polyimide board. The smallest via used will be a finished (i.e., post-plating) 13 mil hole, +/- 0.003", a 30 mil +/- 0.003" pad with a minimum of a 2 mil annular ring specified. This exceeds the NASA specification for both via aspect ratio and minimum annular ring. All boards will be ordered as fully electrically tested by the vendor and complete coupon testing will be performed here at NASA Goddard for the flight units.

The layer stackup is symmetrical with uniform dielectric separation and constructed as follows:

FREE PCB Layer	Layer Material	Layer Name	Contents	Copper Thickness
L1	Rigid Polyimide	Primary Component	Traces	H type 1 oz.
L2	Rigid Polyimide	Flex Signal 2	Traces	H type 1 oz.
L3	Kapton Flex	Flex Signal 3	Traces	RA type 1 oz.
L4	Kapton Flex	Analog Ground	Plane	RA type 1 oz.
L5	Rigid Polyimide	VCC Power	Plane	H type 1 oz.
L6	Rigid Polyimide	Digital Ground	Plane	H type 1 oz.
L7	Kapton Flex	VDD Power	Plane	RA type 1 oz.
L8	Kapton Flex	Flex Signal 8	Traces	RA type 1 oz.
L9	Rigid Polyimide	Flex Signal 9	Traces	H type 1 oz.
L10	Rigid Polyimide	Secondary Component	Traces	H type 1 oz.

The flight FREE printed circuit cards will be handled and assembled as per NASA standard 8739.

FREE Printed Circuit Card (top assy view)



FREE Printed Circuit Card (bottom assy view)

The breadboard FREE layout may be viewed at: http://lhea-glast.gsfc.nasa.gov/acd/electronics/